`timescale 1ns / 1ps

module test\_approx;

// Inputs

reg clk;

reg reset;

reg [15:0] in\_a;

reg [15:0] in\_b;

// Outputs

wire [4:0] shift\_a;

wire [4:0] shift\_b;

wire [15:0] out\_A;

wire [15:0] out\_B;

// Instantiate the Unit Under Test (UUT)

approx\_mul uut (

.clk(clk),

.reset(reset),

.in\_a(in\_a),

.in\_b(in\_b),

.shift\_a(shift\_a),

.shift\_b(shift\_b),

.out\_A(out\_A),

.out\_B(out\_B)

);

always #5 clk = ~clk;

initial begin

// Initialize Inputs

clk = 0;

reset = 0;

in\_a = 0;

in\_b = 0;

#10

in\_a = 16'b0001111111111111;

in\_b = 16'b1111111111111111;

// Wait 100 ns for global reset to finish

#10 $finish;

// Add stimulus here

end

endmodule